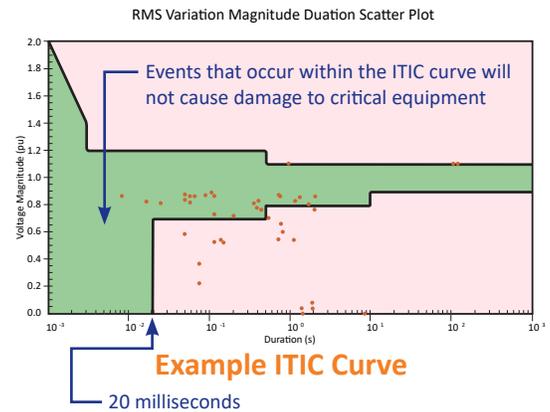## Brief History of ITIC Curves

In 1977 a group called the Computer & Business Equipment Manufacturer's Association (CBEMA) formed with the mission of developing a curve to show the ability of computer equipment to withstand voltage events. This group published a curve as part of IEEE Std 446. In 1996, this group became the Information Technology Industry Council (ITIC), and published the curve still being used today. This curve is meant to represent typical loads and how sensitive the loads are to voltage events. Some loads have been found to be have longer ride-through times and some loads have been found to be less tolerant.

How to Read the Curve

The y-axis displays the percentage of nominal voltage, and the x-axis represents time typically shown using a logarithmic scale. If the RMS voltage is contained within the boundaries the *load will be maintained*. The example to the right shows events plotted both in and out of the boundaries.

RMS Variation Magnitude Duation Scatter Plot

Events that occur within the ITIC curve will not cause damage to critical equipment

Example ITIC Curve

20 milliseconds

LayerZero Products & The ITIC Curve

All LayerZero Power Systems products have on-board power quality analyzers that break down power sources into samples. If the power quality goes out of specification on a source, eSTS will transfer to the alternate source, automatically generating waveform captures and ITIC curves of the event. This data is remotely accessible by connecting to the unit via web browser.

Waveform captures provide a phase-by-phase graph of the voltage/amps over a period of time, and typically requires a well-trained expert to read and interpret the results. ITIC plots do not require an expert analysis, they are simple, easy-to-understand graphs that communicate whether or not connected critical equipment was impacted by power quality events.
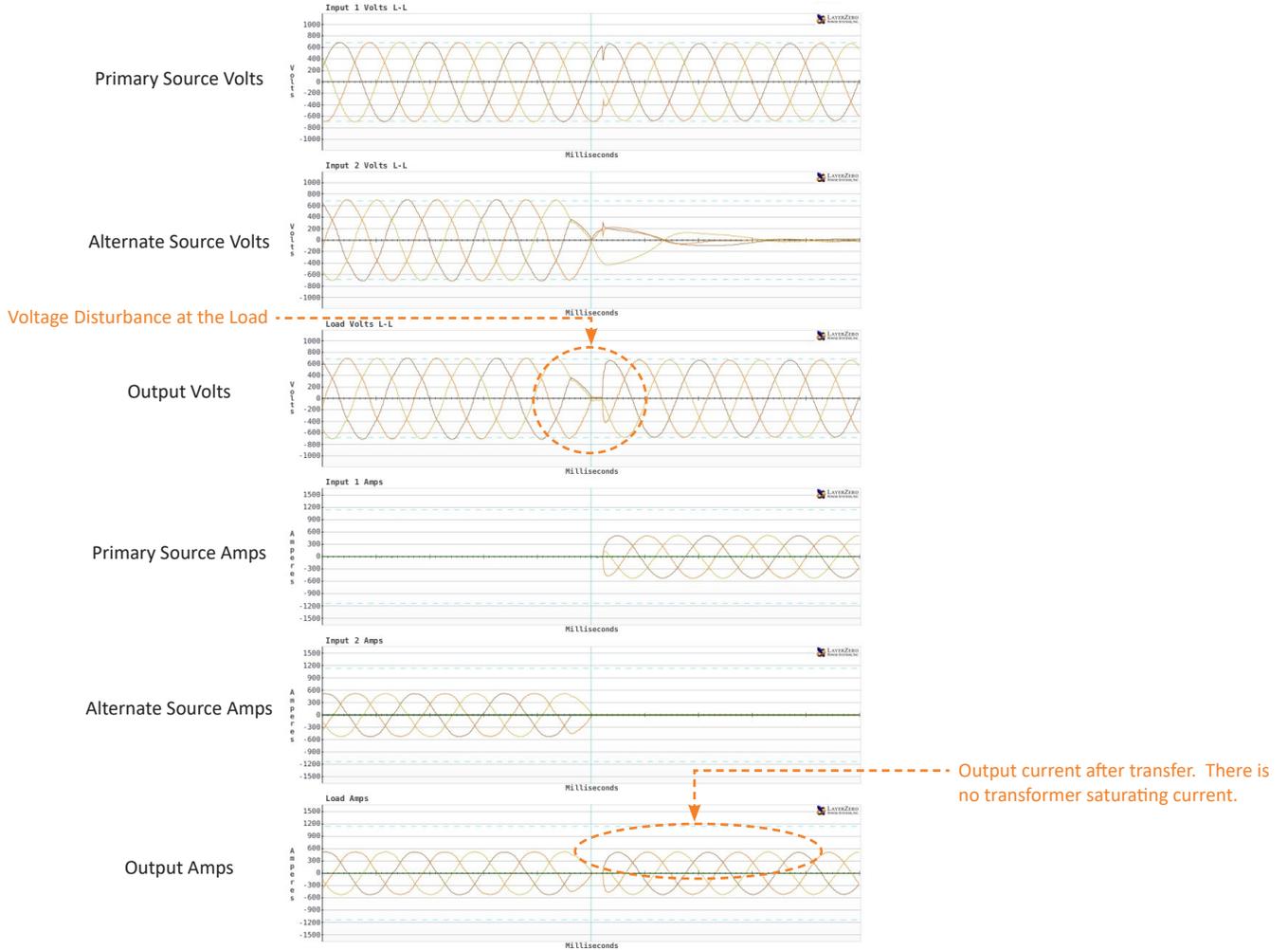
Proving STS Performance

A common critical power distribution system consists of STS systems switching at 480 volts, connected to downstream PDUs with transformers. In critical electrical distribution systems, the phase relationship of two sources sometimes drift apart. When sources are out-of-phase, a ¼ cycle transfer will cause the transformer to draw large inrush currents. These inrush currents could potentially trip upstream overcurrent devices and take down large blocks of critical load. To help mitigate transformer inrush, LayerZero deploys a transfer algorithm called "Dynamic Phase Compensation". This algorithm senses if sources are out-of-phase, and delays the transfer until the perfect moment to switch sources, reducing inrush to practically nothing at all. Utilizing Dynamic Phase Compensation, the transfer time is lengthened. The transfer delay will never impose a complete outage for more than 20 ms. LayerZero provides ITIC plots of the STS output voltage for each transfer event.
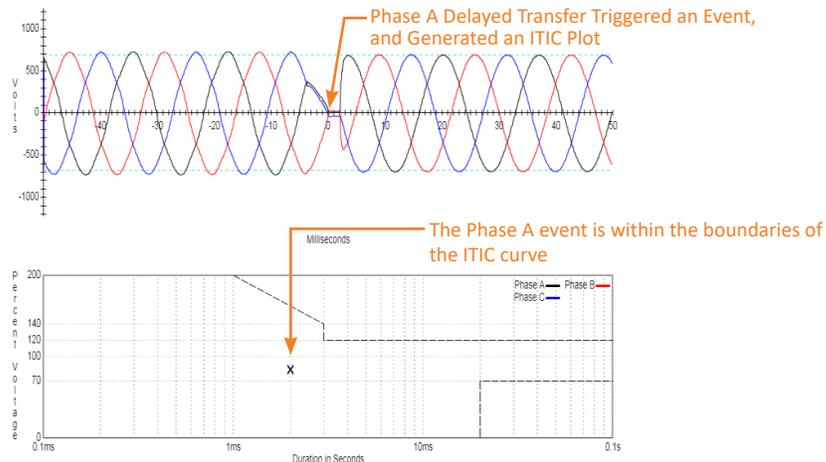
Monitoring & Reporting

All LayerZero products contain an embedded system that continuously monitors the voltage and current of each source and STS output. Any power quality event, such as a source transfer, overcurrent, undercurrent, or overvoltage - will automatically trigger a waveform capture and ITIC plot generation. This provides end-users with the ability to audit the effects of power quality events on all connected LayerZero equipment. For example, if a static transfer switch transfers sources, users will be able to see a timestamped waveform capture and ITIC plot of the event at the STS. The ITIC plot will provide a binary answer regarding the success of the transfer event.

The following "primary to secondary transfer" factory test was performed on a LayerZero 480 V, 800 A, 2 source Static Transfer Switch (STS) connected to two sources 90 degrees out-of-phase. Source 2 breaker was opened, causing the STS to perform an automatic transfer to the primary source. A delayed transfer occurred, causing an event on Phase A, generating an ITIC plot.

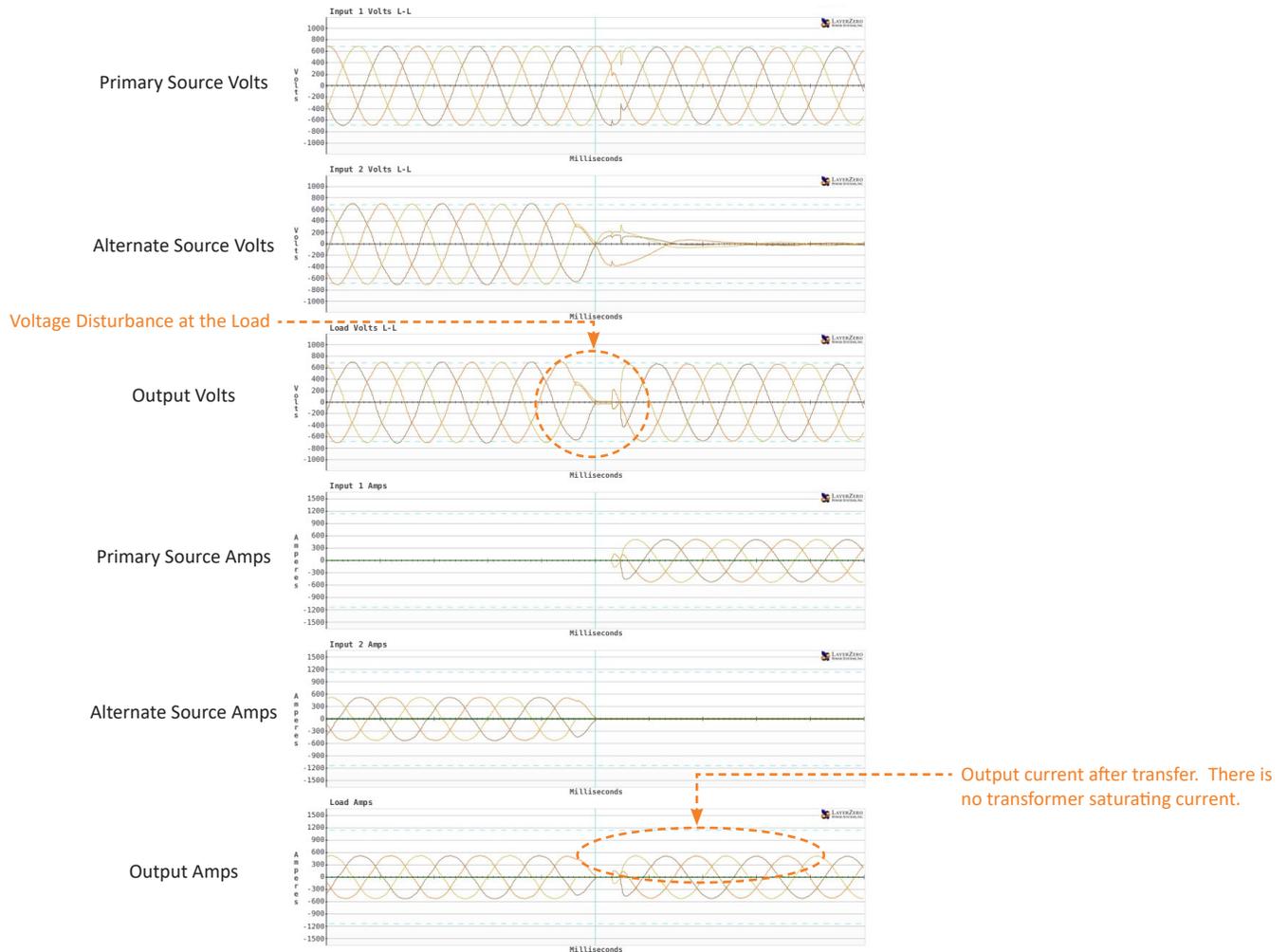### Source 2 to Source 1 Transfer Event, 90 Degrees Out-of-Phase - STS WFC

Primary Source Volts

Alternate Source Volts

Voltage Disturbance at the Load

Output Volts

Primary Source Amps

Alternate Source Amps

Output current after transfer. There is no transformer saturating current.

Output Amps

Source 2 to Source 1 Transfer Event, 90 Degrees Out-of-Phase - STS WFC & ITIC Plot

Phase A Delayed Transfer Triggered an Event, and Generated an ITIC Plot

The Phase A event is within the boundaries of the ITIC curve

Conclusion: Voltage disturbance from the STS transfer event was within the ITIC bounds.

The test below exemplifies LayerZero's "Dynamic Phase Compensation" algorithm in action. In this test, a 480 VAC STS with downstream transformer was connected to two sources 150 degrees out-of-phase. Source 2 breaker was opened, causing the STS to perform an automatic transfer to the primary source. To eliminate transformer inrush, Dynamic Phase Compensation delayed the transfer for approximately three milliseconds, causing events on Phases A, B, and C, automatically generating ITIC plots.

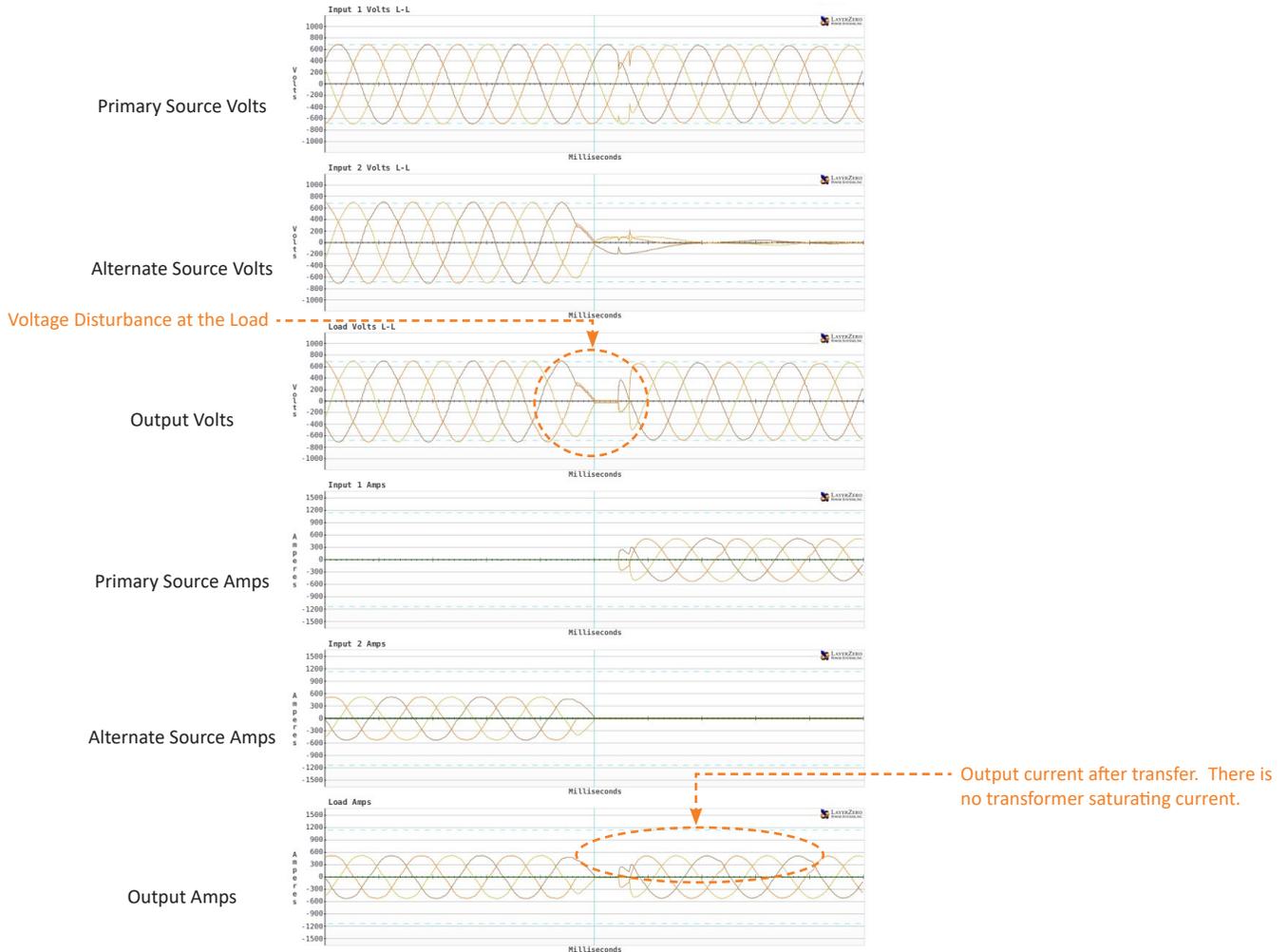## Source 2 to Source 1 Transfer Event, 150 Degrees Out-of-Phase - STS WFC

Source 2 to Source 1 Transfer Event, 150 Degrees Out-of-Phase - STS WFC & ITIC Plot
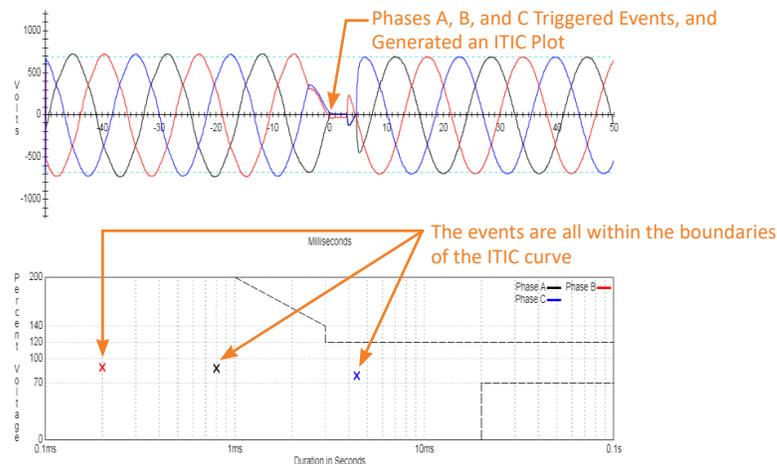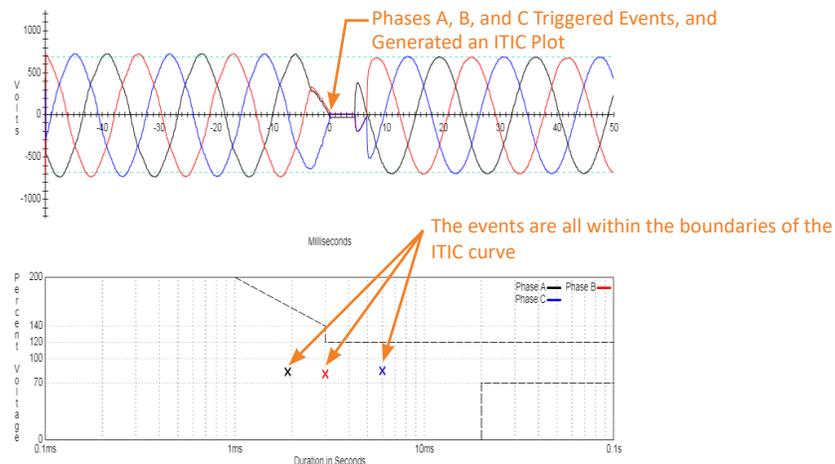

Conclusion: Voltage disturbance from the STS transfer event was within the ITIC bounds.

In the test below, the STS was connected to two sources 180 degrees out-of-phase. While the STS was operating on Source 2, the Source 2 feeder breaker was opened, causing the STS to perform an automatic transfer to the primary source. A delayed transfer occurred, causing events on Phases A, B, and C, automatically generating ITIC plots.

Source 2 to Source 1 Transfer Event, 180 Degrees Out-of-Phase - STS WFC
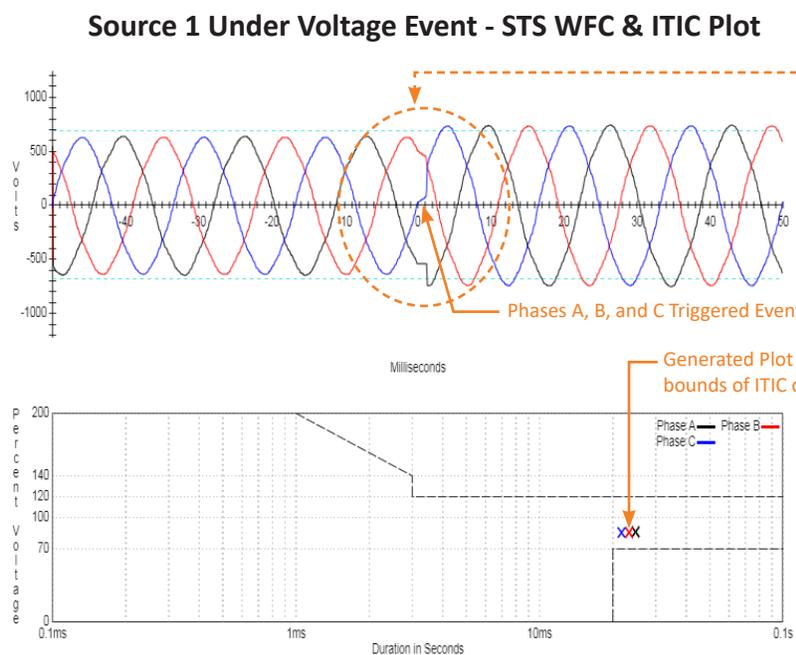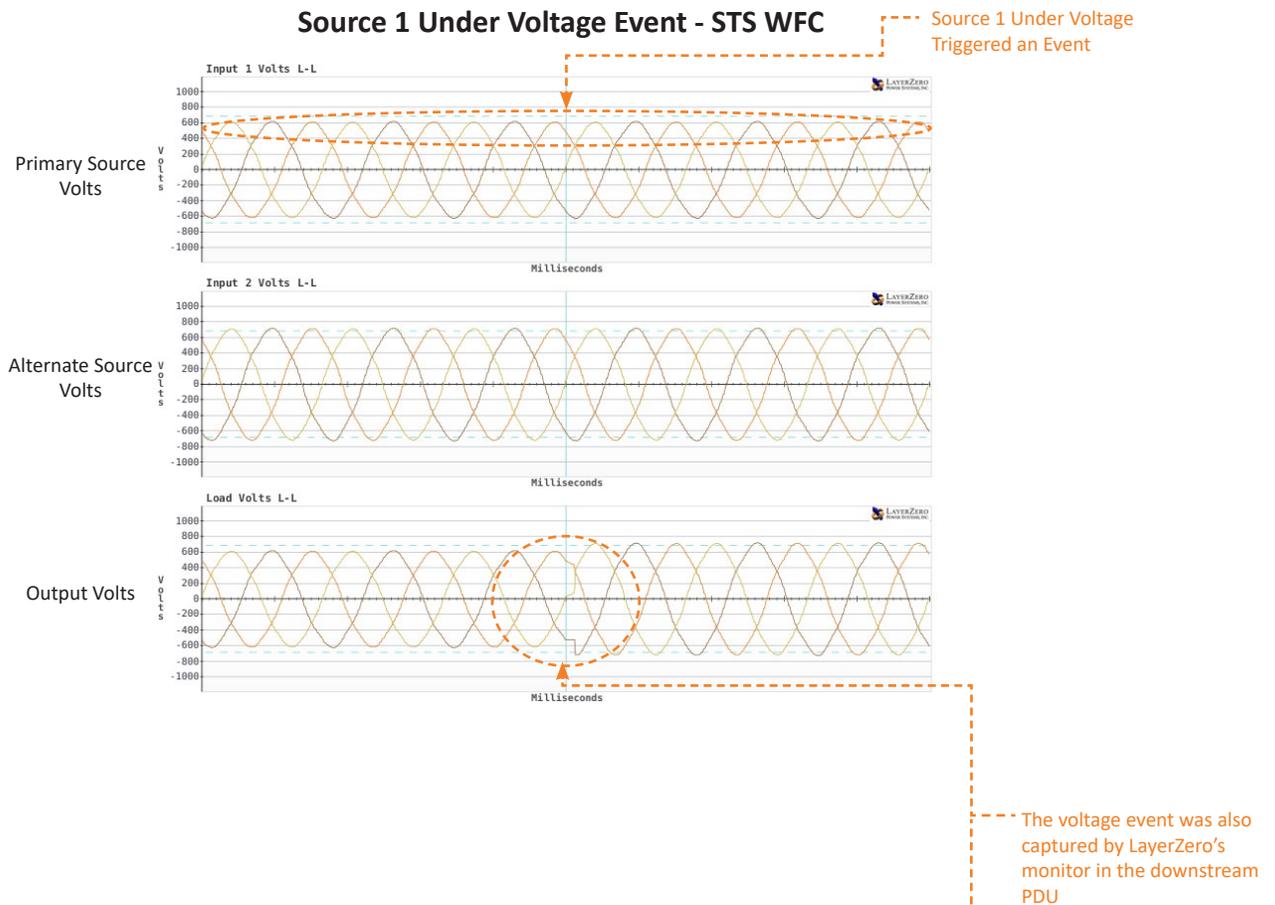

Source 2 to Source 1 Transfer Event, 180 Degrees Out-of-Phase - STS WFC & ITIC Plot
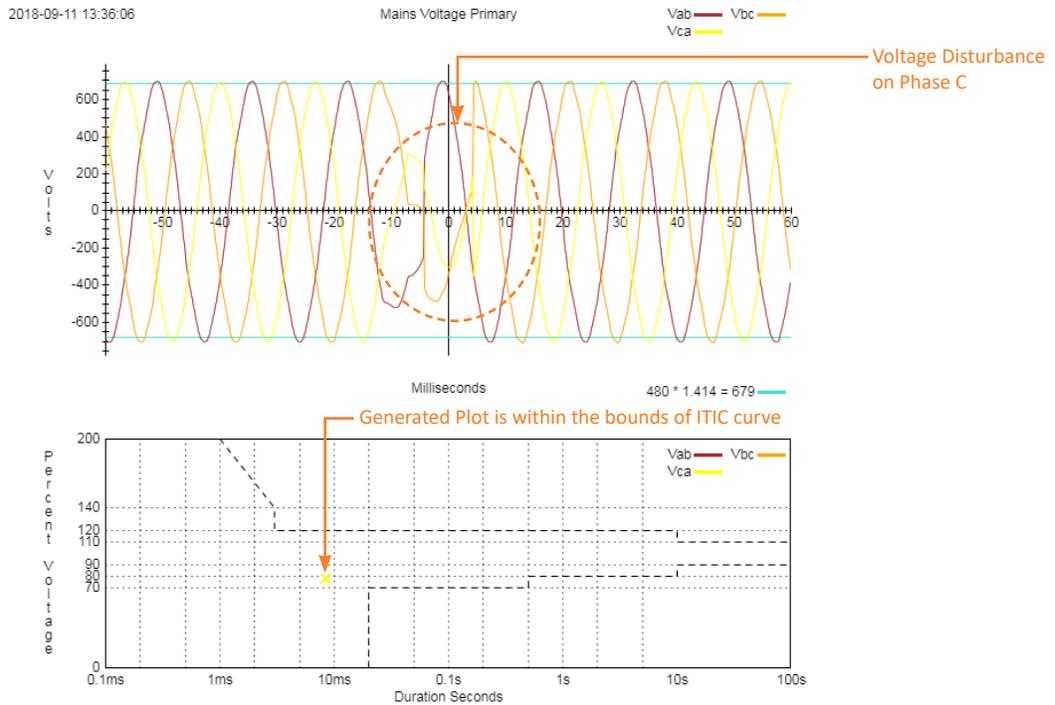

Conclusion: Voltage disturbance from the STS transfer event was within the ITIC bounds.

In the test below, the STS was operating on Source 1, and the sources were in-phase. The voltage was lowered on Source 1 until a transfer occurred, causing the STS to perform an automatic transfer to the primary source. A transfer occurred, causing a events on Phases A, B, and C, generating ITIC plots.

Source 1 Under Voltage Event - STS WFC

Source 1 Under Voltage Triggered an Event

Primary Source Volts

Alternate Source Volts

Output Volts

The voltage event was also captured by LayerZero's monitor in the downstream PDU

Source 1 Under Voltage Event - STS WFC & ITIC Plot

Phases A, B, and C Triggered Events

Generated Plot is within the bounds of ITIC curve

Voltage Disturbance on Phase C - PDU WFC & ITIC Plot

In the test below, the PDU experienced a voltage disturbance on Phase C. This voltage disturbance caused an event on Phase C, generating a waveform capture and ITIC plot.
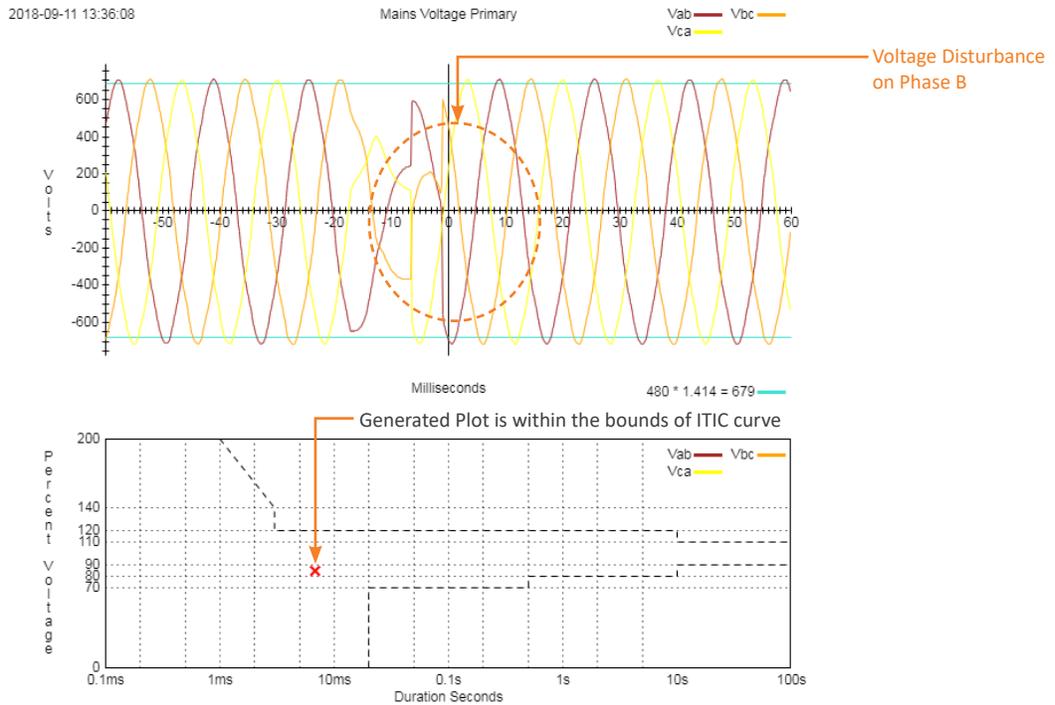

Voltage Disturbance on Phases A and C - PDU WFC & ITIC Plot

In the test below, the PDU experienced a voltage disturbance on Phases A and C. This voltage disturbance caused events on Phases A and C, generating a waveform capture and ITIC plots.
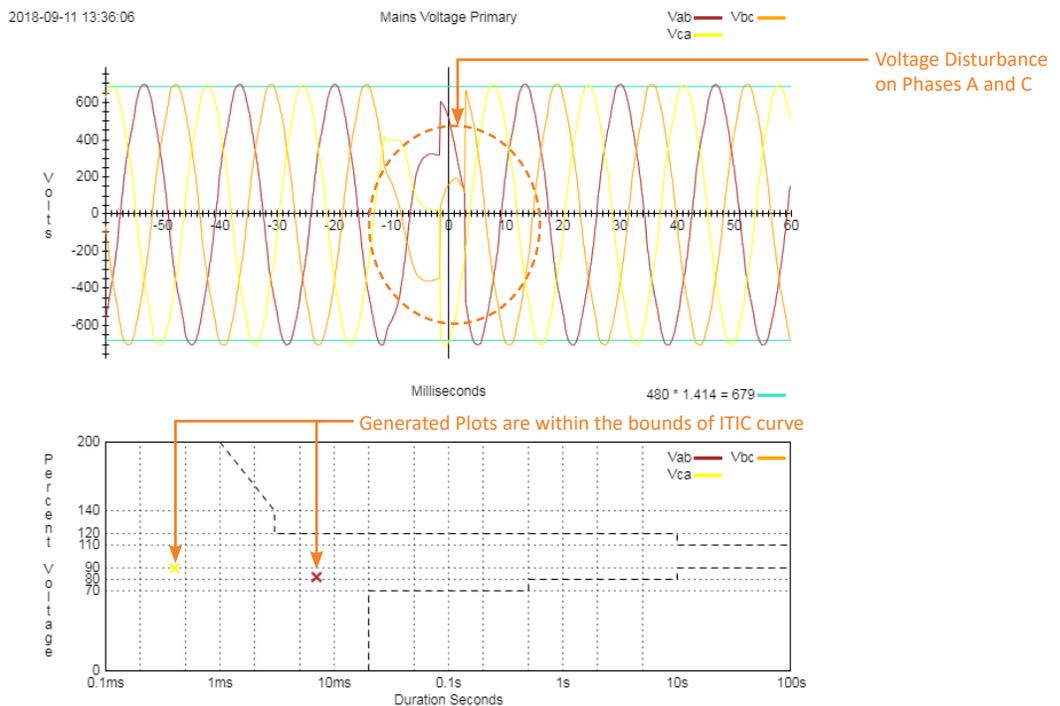
Voltage Disturbance on Phase C - PDU WFC & ITIC Plot

In the test below, the a PDU experienced a voltage disturbance on Phase B. This voltage disturbance caused an event on Phase B, generating a waveform capture and ITIC plot.

Voltage Disturbance on Phases B and C - PDU WFC & ITIC Plot

In the test below, the a PDU experienced a voltage disturbance on Phase C This voltage disturbance caused an event on Phase C, generating a waveform capture and ITIC plots.